REMARKS

I. 35 U.S.C. § 102(b)

In the Office Action, the Examiner has rejected Claims 1-2, 8, 12, 22 and 28 under 35 U.S.C. 35 U.S.C. § 102(b) as allegedly being anticipated by Otake et al., U.S. Patent 5,805,422. The Examiner further rejected Claims 1, 4-5, 9, 11, 21, 24 and 25 as allegedly being anticipated by Fujisawa et al., U.S. Patent 5,801,439. Applicant respectfully disagree.

Applicant claims a semiconductor stacking structure. The stacking structure has a first semiconductor device. A flexible substrate having metal layers for electrical connections is coupled to a bottom surface of the first semiconductor device via the metal layers. The flexible substrate is folded over on at least two sides so as to not overlap and to form flap portions which are coupled to an upper surface of the first semiconductor device. The flap portions cover only a small section of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device. The flexible substrate is used for stacking additional semiconductor devices on the first semiconductor device. Furthermore, by forming the multiple flap portions, the connect density of the stacking structure is increased.

The present invention may be used with any type of device. For example, the stacking structure may be a lead device, an LGA device, a BGA device, and the like.

In contrast, Otake et al. discloses a semiconductor device with a flexible board. The flexible board is used to reduce the area for mounting on a motherboard and to increase the number of terminals for external connections. Nowhere is it disclosed or anticipated that the semiconductor package is a stacked package. Nowhere is it disclosed or anticipated that the folded portions of the flexible board is used to stack additional semiconductor devices on top of the first semiconductor device 101. Furthermore, while Otake shows that the flexible board is folded, as shown in the Figures, the flexible board covers the entire semiconductor device 101. A small opening is provided to inject a mold compound. As stated in the patent application this is cost prohibitive. Applicant's invention solves the cost problem by having the flap sections only cover a portion of the semiconductor device.

Fujisawa et al., discloses a semiconductor device for a stacking arrangement. However, Fujisawa is only used for lead type devices. In fact, as shown in Figure 15-17, the leads of one device are coupled to the leads of another device in order to stack two or more semiconductor lead devices together. Fujisawa cannot be used for other types of devices like Applicant's claimed invention. Furthermore, no where is it disclosed or anticipated in Fujisawa that a flexible substrate is used to stack multiple devices on top of one another. As stated above, Fujisawa uses the leads of the different devices to stack the devices on top of one another and not a flexible substrate as claimed by Applicant.

As the courts have ruled numerous times, anticipation does not exist unless a prior art reference shows each and ever element, united in the same way to perform identical functions (emphasis added). Penn Yan Boats, Inc. v. Sea Lark Boats, Inc., D.C.Fla. 1972, 359 F.Supp. 948, affirmed 479 F.2d 1328, certiorari denied 94 S.Ct. 66. See also, Gillette Co. v. Warner-Lambert Co., D.Mass. 1988, 690 F.Supp. 115, and B.W.B. Controls, Inc. v. U.S. Industries, Inc., E.D.La. 1985, 626 F.Supp. 1553, affirmed 802 F.2d 471. As Applicant has already stated in detail above, Otake et al. and Fujisawa fail to disclose many of the features which Applicant has claimed. Thus, Applicant respectfully submits the amended Claims effectively traverses the Examiner's rejections under 35 U.S.C. §102(b) as allegedly being anticipated by Otake et al or Fujisawa et al. Such action is earnestly solicited.

II. 35 U.S.C. § 102(e)

In the Office Action, the Examiner has rejected Claims 1-2, 4-5, 8, 11-12, 21-22, 24-25 and 28 under 35 U.S.C. 35 U.S.C. § 102(e) as allegedly being anticipated by Chung, U.S. Patent 6,376,769. Applicants respectfully disagree.

As stated above, Applicant claims a semiconductor stacking structure. The stacking structure has a first semiconductor device. A flexible substrate having metal layers for electrical connections is coupled to a bottom surface of the first semiconductor device via the metal layers. The flexible substrate is folded over on at least two sides so as to not overlap and to

form flap portions which are coupled to an upper surface of the first semiconductor device. The flap portions cover only a small section of the upper surface of the first semiconductor device which is smaller than the upper surface of the first semiconductor device. The flexible substrate is used for stacking additional semiconductor devices on the first semiconductor device. Furthermore, by forming the multiple flap portions, the connect density of the stacking structure is increased.

In contrast, Chung uses a flexible interposer. The flexible interposer is used to provide spacing between the stacked semiconductor packages. In order to stack and connect semiconductor devices to one another, Chung requires a plurality of conductive vias. The solder balls will melt during the reflow process thereby coupling one semiconductor device to another via the conductive vias. Chung fails to disclose or anticipate the use of a flexible substrate having metal layers for stacking and coupling two or more semiconductor devices. Thus, Applicant respectfully submits the amended Claims effectively traverses the Examiner's rejections under 35 U.S.C. §102(e) as allegedly being anticipated by Chung. Such action is earnestly solicited.

II. 35 U.S.C. § 103(a)

In the Office Action, the Examiner has rejected Claims 3, 7, 23 and 27 under 35 U.S.C. 35 U.S.C. § 103(a) as allegedly being anticipated by Chung, U.S. Patent 6,376,769. The Examiner has also rejected Claims 6 and 26 under 35 U.S.C. 35 U.S.C. § 103(a) as

allegedly being anticipated by Chung, U.S. Patent 6,376,769 in view of Iwase, U.S. Patent 6,172,418, or Hashimoto et al., U.S. Patent 6,486,544, or Kim et al., U.S. Patent 6,225,688, or Nicewarner, Jr. et al., U.S. Patent 5,776,797. Applicants respectfully disagree.

As stated above, Chung differs from Applicant's claimed invention since Chung uses a flexible interposer. The flexible interposer is used to provide spacing between the stacked semiconductor packages. In order to stack and connect semiconductor devices to one another, Chung requires a plurality of conductive vias. The solder balls will melt during the reflow process thereby coupling one semiconductor device to another via the conductive vias. Chung fails to disclose or anticipate the use of a flexible substrate having metal layers for stacking and coupling two or more semiconductor devices. Thus, Applicant respectfully submits the amended Claims effectively traverses the Examiner's rejections under 35 U.S.C. §103(a). Such action is earnestly solicited.

Applicant respectfully submit that Applicant's claimed invention is deserving of patent protection because it describes a useful and functioning apparatus which is patentably distinguishable over the prior art.

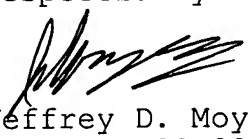
In conclusion, Applicant respectfully submit that this Amendment Letter, including the amendments to the Claims, and in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicant respectfully

submits that he has persuasively demonstrated that the above-identified Patent Application, including Claims 1-12 and 21-28 are in condition for allowance. Such action is earnestly solicited.

If the foregoing does not place the case in condition for immediate allowance, the Examiner is respectfully requested to contact the undersigned for purposes of a telephone interview.

If there are any fees incurred by this Amendment Letter, please deduct them from our Deposit Account NO. 23-0830.

Respectfully submitted,



Jeffrey D. Moy
Reg. No. 39,307
Attorney for Applicants

Weiss, Moy & Harris, P.C.
4204 N. Brown Ave.
Scottsdale, AZ 85251
(480) 994-8888 (Phone)
(480) 947-2663 (Fax)

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